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Thermal Stress Mapping of Power Semiconductors in H-bridge Test Bench

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***Abstract* – As thermal stress of the power semiconductor is an important indicator for reliable power converter operation, the mapping of the junction temperature is becoming crucial need. In this paper, the loss dissipation and thermal stress of the power semiconductor are investigated in the universal H-bridge test bench. It starts with its basic operation principle. Based on the loss and thermal model of the power semiconductor, dominating factors (e.g. power factor, loading current amplitude, fundamental frequency, and switching frequency) impact on the loading stress of the power semiconductors are considerably investigated. Finally, the junction temperature of the power device in terms of the mean vale and temperature swing is verified in PLECS simulation and experimental setup.**

I. INTRODUCTION

Reliability and lifetime prediction of power converters have been a major research topic in the last few decades, especially for renewable energy applications [1], [2]. According to an industrial survey presented in [3], power semiconductor failures are a major concern for reliability of power converter. The main failures in power semiconductors are caused by thermomechanical fatigue, and thus thermal analysis of the power converter is essential for reliability testing in various applications.

Temperature cycling and power cycling are the two most common thermal acceleration test used in assessing the reliability of power device. In the temperature cycling, components are periodically moved between a cooling chamber and a heating chamber, where components are passively heated up. During the power cycling test, components are actively heated up by losses produced in the power semiconductor and cooled down with the aid of cooling equipment. The power device can be heated only by the conduction loss, which is named as the dc power cycling [4]. Alternatively, both the conduction loss and switching loss induce the thermal cycling, which is known as the ac power cycling [5]. As the ac power cycling generates more realistic condition compared to the typical power converter, some research efforts focus on this H-bridge circuit [6], [7]. However, the operation principle of this configuration is not well described. Moreover, the relationship between the loading condition and the junction temperature of the power semiconductor is not accurately established. In order to fill up this research gap, the loss dissipation and thermal stress are considerably investigated at various loading conditions.

The structure of the paper is as follows. Section II introduces the basic operation principle of H-bridge circuit. Section III describes and evaluates the loss and thermal models of the power semiconductor at various loading conditions. Section IV verifies loss dissipation and junction temperature the by PLECS simulation and experimental result. Some conclusions are drawn in Section V accordingly.

II. OPERATION PRINCIPLE OF H-BRIDGE CIRCUIT

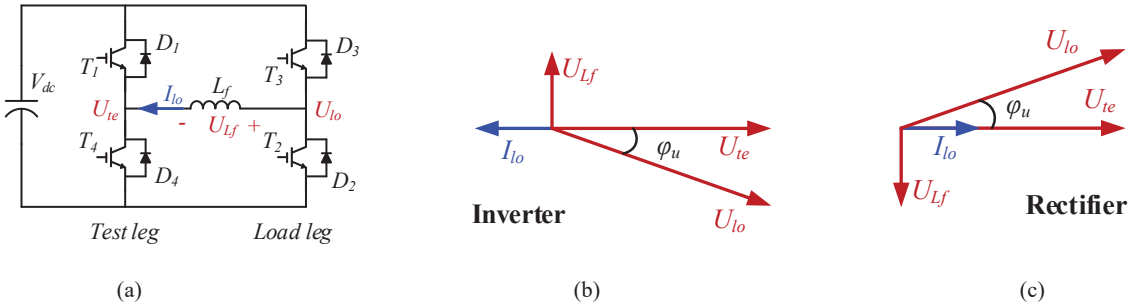
For the grid-tied converter used in the renewable energy systems, the loading of the power devices is dominated by the grid requirements (e.g. active and reactive power). In respect to the power converter applied in generator/motor control, the generated current is tightly dependent upon the machine characteristic. Thus, regardless of the converter applications, its loading can be simply considered as a controlled current source.

A single-phase H-bridge circuit is shown in Fig. 1(a), which is consisted of a test leg and a load leg. An inductor in between is used to eliminate the Pulse-Width Modulation (PWM) harmonics. The test leg provides the reference voltage, while the load leg imitates the loading feature, supplying resistive, inductive or capacitive feature. Consequently, the current flowing through the test leg can be regulated freely. According to the Kirchhoff voltage law, the relationship between the output voltage of the test leg U_{te} and the load leg U_{lo} can be found,

$$U_{te} = U_{lo} + U_{Lf} \tag{1}$$

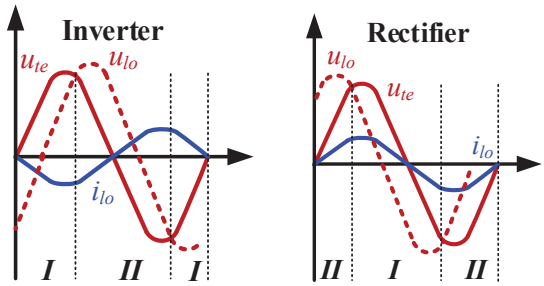
where U_{Lf} is the voltage drop across the filter inductor L_f.

For typical operation conditions, the converter operating in the inverter mode and the rectifier mode are shown in Fig. 1(b) and (c). In the case of the inverter mode, the loading current I_{lo} is in the opposite with the reference voltage U_{te}. The amplitude of the load voltage U_{lo} becomes slightly higher and lags reference voltage with φ_u. Similarly, in the case of the rectifier mode, the loading current is in phase with the reference voltage, which results in the leading load voltage.



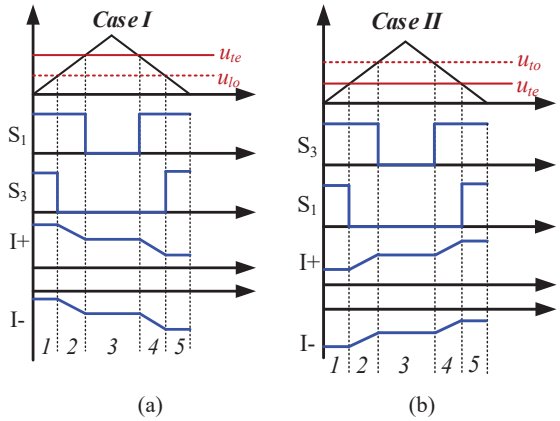
(a) (b) (c)

Fig. 1. Configuration and phasor diagram between test leg and load leg. (a) Single-phase H-bridge circuit. (b) Phasor diagram in the case of inverter mode. (c) Phasor diagram in the case of rectifier mode.



(a) (b)

Fig. 2. Relationship among loading current, voltage of load leg and test leg. (a) Inverter mode. (b) Rectifier mode.



(a) (b)

Fig. 3. Switching pattern of test leg and loading current. (a) Testing voltage is higher than loading voltage. (b) Testing voltage is lower than loading voltage.

Within a fundamental period, the loading current, output voltage of the load leg and test leg are graphically shown in Fig. 2. It can be seen that, both the inverter mode and rectifier mode includes two cases. The modulated test voltage is higher than the load voltage in the case I, while the test voltage is lower than the load voltage in the case II.

Generally, either the bipolar or the unipolar modulation approach is adopted in the single-phase converter [8]. For the bipolar modulation, the inverter output voltage contains the positive and negative dc-bus voltage by activating the diagonal switches simultaneously. For the unipolar modulation, by control the diagonal switches separately, the inverter output voltage includes the positive dc-bus voltage and zero in the period of positive cycle, while it contains the negative dc-bus voltage and zero in the period of negative cycle. Different from the previous methods, the modulation strategy for the test and load legs is illustrated in Fig. 3, where the same carrier and various modulated voltage are used to generate the switching patterns in two legs. The switching patterns of the upper switches of test leg S_1 and load leg S_3 are depicted. If the driving signal of S_1 is on, the conduction of the IGBT T_1 or the freewheeling diode D_1 is dependent on the direction of the loading current. As a result, the stages with the positive current I+ and negative current I- can be divided.

III. Loss Dissipation and Junction Temperature of Power Devices

By knowing the current distribution between the IGBT and freewheeling diode within a fundamental period, their loss dissipation can be calculated analytically. According to the thermal impedance of the power devices and cooling method, the junction temperature can be estimated as well.

A. Loss dissipation

Under steady-state operation, the loading current flowing through the upper IGBT T_1 and lower diode D_4 is described in Fig. 4. Due to the direction of the loading current, both the IGBT and the diode conducts only a half of the fundamental period. Moreover, it can be inferred that the loading of the upper and lower power semiconductor are identical because of the symmetrical feature. As a result, the loss dissipation of T_1 and D_4 is in focus. Within a switching period, as the loading current commutes from D_4 to T_1 once, the conduction loss and switching loss exist in both the IGBT and the diode. Due to the fact that the sinusoidal loading current induces different power loss every switching period, the power loss can be calculated within a fundamental period in order to have the constant value.

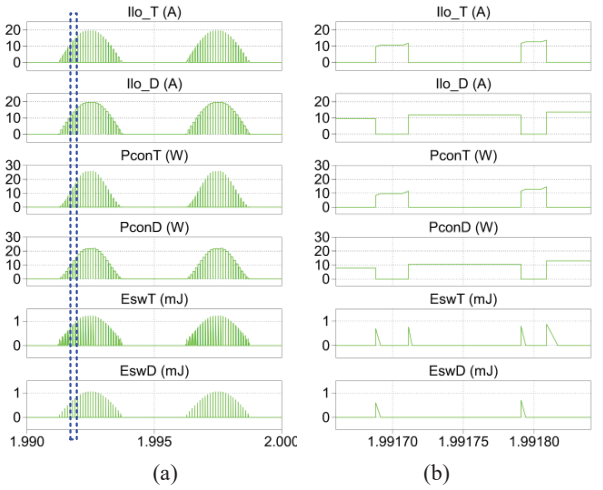


Fig. 4. Schematic diagram of the loss calculation. (a) Operation under steady-state. (b) Zoom-in part.

The conduction loss of the IGBT P_{conT} can be calculated as,

$$\mathrm{P}_{conT} = \frac{1}{T_1}\int_0^{\frac{T_1}{2}} V_{CE}(\mathrm{t})\cdot i_{lo}(\mathrm{t})\cdot d(\mathrm{t})dt \tag{2}$$

where T_1 denotes the fundamental period, V_{CE} denotes the on-state voltage of the IGBT, i_{lo} denotes the loading current, and d denotes the duty cycle.

Suppose the displacement angle between the loading current and modulated voltage φ_u, and the linear approximation of the IGBT forward characteristics (initial on-state voltage drop V_{CE0} and equivalent resistor r_{CE}), the conduction loss of the IGBT can be deduced by,

$$P_{conT} = \frac{1}{2}\left(\frac{1}{\pi}\mathrm{V}_{CE0}\, I_m + \frac{1}{4}\mathrm{r}_{CE}\cdot I_m^{\,2}\right) + M\cos\varphi_u\left(\frac{1}{8}\mathrm{V}_{CE0}\, I_m + \frac{1}{3\pi}\mathrm{r}_{CE}\cdot I_m^{\,2}\right) \tag{3}$$

where I_m denotes the amplitude of the loading current, and M denotes the modulation index, which equals the converter output voltage over half of the dc-bus voltage.

Similarly, the conduction loss of the diode P_{conD} can be calculated as,

$$\mathrm{P}_{conD} = \frac{1}{T_1}\int_0^{\frac{T_1}{2}} V_F(\mathrm{t})\cdot i_{lo}(\mathrm{t})\cdot(1-d(\mathrm{t}))dt \tag{4}$$

where V_F denotes the on-state voltage of the freewheeling diode. It can be noted that the lower diode conducts if its driving signal is high.

Assuming the linear approximation of the diode forward characteristics (initial on-state voltage drop V_{F0} and equivalent resistor r_F), the conduction loss of the diode can be deduced by,

$$P_{conD} = \frac{1}{2}\left(\frac{1}{\pi}\mathrm{V}_{F0}\, I_m + \frac{1}{4}\mathrm{r}_F\cdot I_m^{\,2}\right) - M\cos\varphi_u\left(\frac{1}{8}\mathrm{V}_{F0}\, I_m + \frac{1}{3\pi}\mathrm{r}_F\cdot I_m^{\,2}\right) \tag{5}$$

As the turn-on energies E_{on} and turn-off energies E_{off} of the IGBT can be described as a polynomial function,

$$E_{swT}(\mathrm{t}) = E_{on}(\mathrm{t}) + E_{off}(\mathrm{t}) = \frac{V_{dc}}{V_{dc}^{\,*}}\left(a_T + b_T I_m(\mathrm{t}) + c_T I_m^{\,2}(\mathrm{t})\right) \tag{6}$$

so the switching loss P_{swT} can be calculated within a fundamental period,

$$\mathrm{P}_{swT} = \frac{1}{T_1}\sum E_{swT}(\mathrm{i}) = f_{sw}\frac{V_{dc}}{V_{dc}^{\,*}}\left(\frac{a_T}{2} + \frac{b_T}{\pi}I_m + \frac{c_T}{4}I_m^{\,2}\right) \tag{7}$$

where f_{sw} denotes the switching frequency, V_{dc} denotes dc-bus voltage, and $V_{dc}^{\,*}$ denotes the dc-bus voltage at the testing condition.

The recovery energy of the diode E_{rr} can be described as a polynomial function,

$$E_{swD}(\mathrm{t}) = E_{rr}(\mathrm{t}) = \frac{V_{dc}}{V_{dc}^{\,*}}\left(a_D + b_D I_m(\mathrm{t}) + c_D I_m^{\,2}(\mathrm{t})\right) \tag{8}$$

The switching loss of the diode P_{swD} can be deduced as follows,

$$\mathrm{P}_{swD} = \frac{1}{T_1}\sum E_{swD}(\mathrm{i}) = f_{sw}\frac{V_{dc}}{V_{dc}^{\,*}}\left(\frac{a_D}{2} + \frac{b_D}{\pi}I_m + \frac{c_D}{4}I_m^{\,2}\right) \tag{9}$$

B. Junction temperature estimation

Thermal stress of the power devices is usually determined by the thermal parameters of the power module itself (from junction to case), and the Thermal Integrate Material (TIM), and the cooling method. A typical thermal model of the power module is graphically depicted in Fig. 5. It can be seen that the power switches share the common cooling system, since these power devices are located in the same housing of the IGBT module.

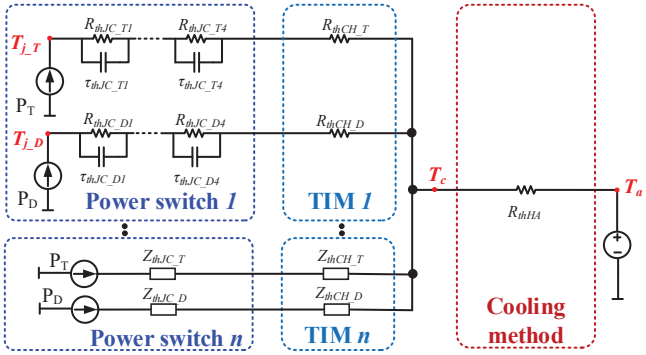


Fig. 5. Thermal model of power semiconductor for thermal cycling caused by the fundamental frequency.

Generally, the thermal time constant of the cooling system is from dozens of seconds to hundreds of seconds, while the thermal time constant of the power device is hundreds of milliseconds. On the other hand, the maximum fundamental period of the converter current is around several seconds, which implies that the thermal cycling caused by the cooling can almost be neglected [9], [10]. As a result, for the steady-state, the thermal model of the cooling method will only affect the mean junction temperature, but not disturb the junction temperature fluctuation.

Consequently, the mean junction temperature T_{jm} and the junction temperature fluctuation dT_j can be calculated as,

$$T_{jm\_T/D} = P_{T/D} \cdot (\sum_{i=1}^{4} R_{thJC\_T/D(i)} + R_{thCH\_T/D}) + n \cdot (P_T + P_D) \cdot R_{thHA} + T_A \quad (10)$$

$$dT_{j\_T/D} = 2P_{T/D} \cdot \sum_{i=1}^{4} R_{thJC\_T/D(i)} \cdot \frac{(1 - e^{-\frac{t_{on}}{\tau_{thJC\_T/D(i)}}})^2}{1 - e^{-\frac{t_p}{\tau_{thJC\_T/D(i)}}}} \quad (11)$$

In Eq. (10), R_{thJC} , R_{thCH} , R_{thHA} denote the thermal resistance from the junction to case of the power module, the TIM, and the cooling method, respectively. Subscripts T and D denote the IGBT and the freewheeling diode, where subscripts i denotes four-layer Foster structure for power module. P is the power loss of each power semiconductor, n is the number of the power switches associated with the heatsink, and T_A is the ambient temperature. In Eq. (11), t_p denotes the fundamental period of the current, t_{on} denotes a half of fundamental period, and τ denotes the thermal time constant of each Foster layer.

IV. Thermal Stresses of Power Devices at Various Loading Conditions

In this section, the factors that affect the thermal loading of the power devices are first to investigated. Then, their loss dissipation and thermal stresses are analytically calculated and compared with the simulation and experimental results.

A. Dominating factors for device loading

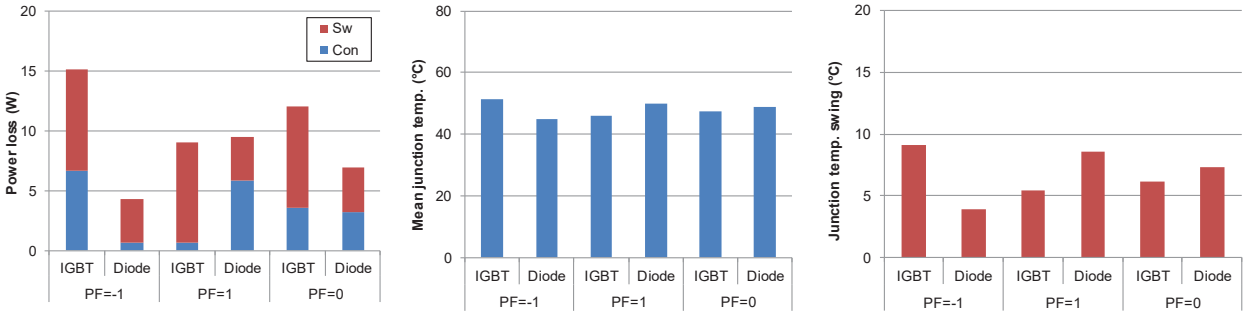
The key parameters of the power converter are listed in Table I, where a 1200 V/50 A power module with a maximum junction temperature of 150 °C is selected for both the test and load leg. The converter operating at the inverter mode, i.e. Power Factor (PF) equals -1, is regarded as the rated condition. Moreover, the rated current, fundamental frequency, and switching frequency are summarized in Table I as well. As the advantage of this configuration is able to emulate various loading conditions, different power factor, peak current, fundamental frequency, and switching frequency impacts on the loss dissipation and thermal stress of the power devices will be evaluated.

In the case of various power factors, the PF of -1, 1, and 0 indicates the converter operating as the inverter, the rectifier, and the reactive power generator. The loss dissipation and thermal stress of the IGBT and the diode is summarized in Fig. 6. It is noted that the conduction loss changes between the IGBT and the diode, while the switching loss keeps the same. The conduction loss of the IGBT is dominant in the inverter mode, but the conduction loss of the diode determines in the rectifier mode. As a result, the mean junction temperature and the junction temperature swing of the IGBT and the diode changes in according with their loss dissipation. By using the similar approach, various current amplitude, fundamental frequency, switching frequency impact on loss dissipation and thermal stress of the power semiconductor can be investigated.

Table I

Parameters and Rated Condition of Converter

Rating of power device	1200 V/50 A
Filter inductor	1.5 mH
DC-link voltage	400 V
Rated power factor	-1
Rated peak current I_{lo}	20 A
Rated fundamental frequency f_l	10 Hz
Rated switching frequency f_{sw}	10 kHz



(a) (b) (c)

Fig. 6. Various power factor (PF) impacts. (a) Loss dissipation. (b) Mean junction temperature. (c) Junction temperature swing.

B. Simulation and experimental verification

Consistent with the converter parameters listed in Table I, the simulation can be carried out by using PLECS. At the inverter mode and rectifier mode, the power loss and junction temperature of the IGBT and the diode are shown in Fig. 7(a) and (b), respectively. In the case of the inverter mode, the IGBT is the most stressed. It can be observed that the loss dissipation consumes 15.1 W, and the junction temperature fluctuates between 46.8 and 57.7 °C. Nevertheless, the diode is the most stressed under the rectifier mode, with the power loss of 9.5 W and the temperature swing of 10.5 °C.

The simulated loss and thermal loading of the power semiconductor are compared with the analytical calculation as listed in Table II. It is evident that they well agree with each other. In order to verify the accuracy of the loss and thermal calculation, the operation conditions with various power factor,

loading current, fundamental frequency, and switching frequency are again simulated. As can be seen from Table II, the simulated power loss and mean junction temperature of the power devices match the calculation. However, the simulated junction temperature is slightly higher than the calculation, as the constant power loss within the fundamental frequency is assumed in the calculation.

Table II

COMPARISON BETWEEN CALCULATION AND SIMULATION FOR LOSS AND THERMAL STRESS OF POWER DEVICES

		IGBT			Diode		
		P_{loss} (W)	T_{jm} (°C)	dT_j (°C)	P_{loss} (W)	T_{jm} (°C)	dT_j (°C)
Rated condition	Cal.	15.1	51.4	9.1	4.3	45.0	3.9
	Sim.	15.1	52.3	10.9	4.3	45.2	4.2
PF=1	Cal.	9.0	46.1	5.4	9.5	49.9	8.6
	Sim.	9.0	46.4	6.1	9.5	50.8	10.5
I_{lo}=5 A	Cal.	4.0	28.6	2.4	1.5	27.3	1.3
	Sim.	4.0	28.7	2.6	1.4	27.3	1.4
f_1=50 Hz	Cal.	15.1	51.4	2.5	4.3	45.0	1.1
	Sim.	15.1	51.6	2.9	4.3	45.1	1.1
f_{sw}=5 kHz	Cal.	10.9	42.0	6.5	2.4	36.6	2.2
	Sim.	10.9	42.7	8.1	2.4	36.7	2.4

Note: "Rated condition" indicates PF=-1, I_{lo}=20 A, f_1=10 Hz, f_{sw}=10 kHz. "Cal." and "Sim." indicate calculation and simulation results.

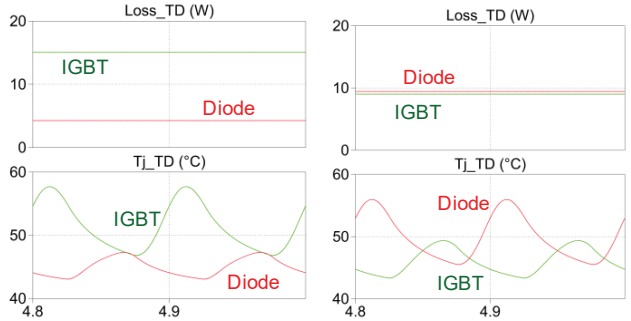


Fig. 7. Loss dissipation and junction temperature of IGBT and diode. (a) Inverter mode. (b) Rectifier mode.

In respect to the experimental setup, the control scheme of the test leg and the load leg is shown in Fig. 8. By using the open-loop control, the driving signal of the test leg is generated from the required voltage profile. However, the driving signal of the load leg is produced by using the closed-loop control of the loading current. As the power module with three legs are applied, the similar control strategy can be transferred to the other two phases based on the delayed starting angle of the reference voltage. The photo of the experimental setup is shown in Fig. 8(b). It is worthwhile to mention that the control scheme is realized by TI Digital Signal Processor (DSP) TMS320F28335, and the OpSen thermal fiber is adopted to measure the junction temperature in the open power module.

As show in Fig. 9, the converter can operate in either the inverter mode or the rectifier mode. In the case of the inverter mode, the loading current should be in phase with the phase voltage. Since the phase voltage cannot be directly measured, the line voltage is presented, which leads to phase voltage 30°.

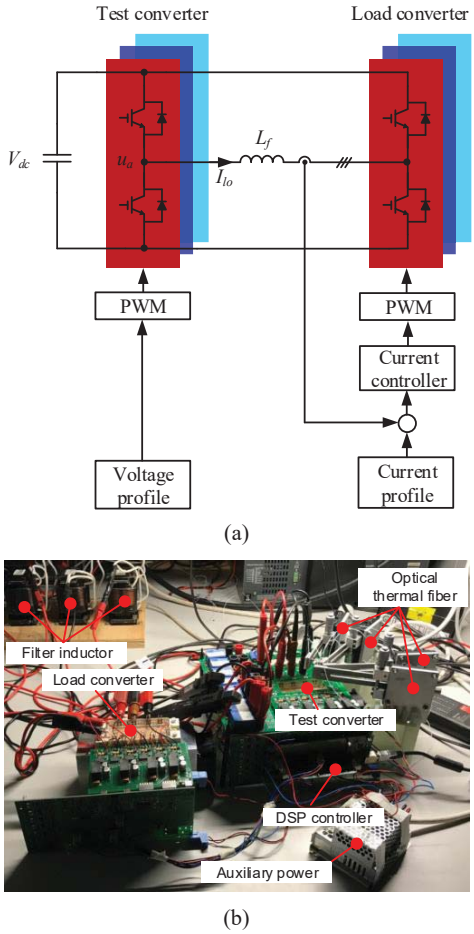
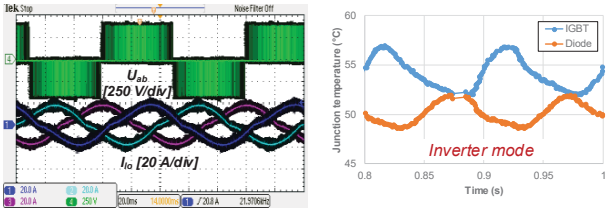
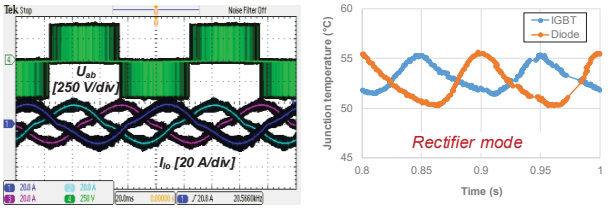


Fig. 8. Experimental setup with three-phase H-bridge circuit. (a) Control block diagram. (b) Photo of experimental setup.



(a)



(b)

Fig. 9. Experimental results in terms of the loading current and junction temperature of power semiconductors. (a) Inverter mode. (b) Rectifier mode.

As a result, it can be inferred that the loading current is in phase with the phase voltage. In respect to the junction temperature, it is noted that the temperature is fluctuated with the fundamental frequency of 10 Hz. Moreover, the IGBT is more stressed compared to the diode. In the case of the rectifier mode, it is evident that the loading current is out of phase with the phase voltage. Besides, the junction temperature of the diode is higher than the IGBT, which is consistent with the analytical calculation.

V. Conclusion

In this paper, an H-bridge circuit is used to emulate the power converter operating at various loading conditions. It starts with the operation principle, when the converter works at the positive and negative unity power factor. Then, the loss and thermal stresses of the power semiconductors are described in detail. Dominating factors like power factor, loading current amplitude, fundamental frequency, and switching frequency impact on the loading stress of the power semiconductors are considerably investigated, which are compared with PLECS simulation. Finally, the junction temperature of the power semiconductors is measured in the experimental setup, which further verifies their loss and thermal models.

References

[1] F. Blaabjerg, and K. Ma, "Future on power electronics for wind turbine systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 139-152, Sept. 2013.

[2] H. Wang, M. Liserre, F. Blaabjerg, P. Rimmen, J. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 97-114, Mar. 2014.

[3] S. Yang, A. T. Bryant, P. A. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry based survey of reliability of power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May 2011.

[4] L. R. GopiReddy, L. M. Tolbert, and B. Ozpineci, "Power cycle testing of power switches: a literature survey," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2465–2473, May 2015.

[5] U. Choi, S. Jørgensen, and F. Blaabjerg, "Advanced accelerated power cycling test for reliability investigation of power device modules," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8371-8386, Dec. 2016.

[6] Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, "Thermally compensated discontinuous modulation strategy for cascaded H-bridge converters," *IEEE Trans. on Power Electronics*, vol. 33, no. 3, pp. 2704-2713, Mar. 2018.

[7] C. v. d. Broeck, H. Zeng, R. D. Lorenz, and R. W. d. Doncker, "A test bench for thermal characterization of IGBT power modules over mission profiles," *in Proc. of PCIM Europe 2018*, pp. 1-8, 2018.

[8] B. Ji, J. Wang, and J. Zhao, "High-efficiency single-phase transformerless PV H6 inverter with hybrid modulation method," *IEEE Trans. on Industrial Electronics*, vol. 60, no. 5, pp. 2104-2115, May 2013.

[9] D. Zhou, and F. Blaabjerg, "Optimized demagnetizing control of DFIG power converter for reduced thermal stress during symmetrical grid fault," *IEEE Trans. on Power Electronics*, vol. 33, no. 12, pp. 10326-10340, Dec. 2018.

[10] D. Zhou, F. Blaabjerg, M. Lau, and M. Tonnes, "Optimized reactive power flow of DFIG power converters for better reliability performance considering grid codes," *IEEE Trans. on Industrial Electronics*, vol. 62, no. 3, pp. 1552-1562, Mar. 2015.